REMARKS

Claims 2-4, 7-11, 15, 17-19, 21, and 25-50 are pending in the present application after this amendment cancels claims 1, 5, 6, 12-14, 16, 20, and 22-24 and adds new claims 45-50. Claims 2-4, 7, 8, 11, 15, 17-19, 21, 25, 34, 35, 37, 39, 41, 43, and 44 and the specification have been amended to correct typographic errors, to change claim dependencies, and/or to clarify the subject matter recited therein. No new matter is added by the amendments and new claims, which find support throughout the specification and figures. As this Amendment is filed contemporaneously with a Request for Continued Examination, it is respectfully requested that the claim amendments be entered. In view of the amendments and the following remarks, favorable reconsideration of this case is respectfully requested.

Applicants note with appreciation that the Examiner has allowed claims 9 and 10 and determined that claims 7, 8, 15, 17, 21, and 25-44 are directed to allowable subject matter. Applicants hereby acknowledge the Examiner's reasons for indication of allowable subject matter. Applicants respectfully note that there may be additional reasons for allowing these claims that have not been specifically cited in addition to or instead of the cited reasons. Additionally, claim 25 has been amended into independent form, and therefore, claim 25, as well as claims 26-44 which depend therefrom, are now in condition for allowance.

The Examiner objects to the specification based on an informality, which has been amended as suggested by the Examiner. Therefore it is respectfully requested that the objection to the specification be withdrawn.

Claims 2-4, 11, 18, and 19 (claim 1 having been canceled) are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,661,690 to Moriarty et al. (hereinafter Moriarty). Applicants respectfully traverse.

Claim 2 relates to a memory module comprising a plurality of memory devices, which share a bus line, on a board. In claim 2, the bus line connects terminals of the plurality of memory devices in a stubless configuration and an end of the bus line is terminated, and ***at least a part of the bus line is a strip line***.

Applicants respectfully submit that Moriarty does not disclose, or even suggest, the feature of memory devices connected to a bus line in a stubless configuration in which a part of the bus line is a strip line.

Moriarty apparently discloses a circuit arrangement in which the wiring runs along the long side of the memory module (i.e., in parallel with the connector), and the terminals are disposed on one side or both sides of the module. The input terminals and output terminals are concentrated on one of the right or left side of the module, thus resulting in a small allowable number of wirings. In other words, the allowable number of wiring are limited.

In contrast to Moriarty, the present invention provides a wiring arrangement that runs along (in parallel with) the short side of the module (i.e., at right angles with the connector), and the terminals are disposed on both (upper and rear) surfaces of the module. By this arrangement, the input terminals and the output terminals of the wirings can be disposed broadly over the entire right and left sides, thereby enabling disposition of a far larger number of wirings. Therefore, it is apparent that Moriarty does not disclose or suggest, memory devices connected to a bus line in a stubless configuration, and therefore Moriarty does not anticipate claim 2.

However, in the interest of expediting prosecution, claim 1 has been canceled and claim 2 has been amended into independent form and including the features of claim 1. The Office Action asserts that Moriarty discloses that at least a part of the bus line is a strip line at element 104.

(Office Action; page 3, lines 1-2). However, element 104 in Moriarty is bus entry region. (Moriarty; col. 8, lines 6-7). In contrast, the Specification of the present application states:

> In a bus configuration according to the present invention, ***a stubless memory bus which has a termination and is directly mounted on a board is built on a memory module (1 in FIG. 4) using a strip line.*** The memory module (1) is mounted on a motherboard (3 in FIG. 4), on which a memory controller (2 in FIG. 4) is mounted, through a connector (4 in FIG. 4). The memory module (1) has a bus line for one data signal. The bus line connects the terminals of a plurality of memories (115) in a stubless configuration, that is, in a single stroke, using a strip line with its end terminated on the memory module (1). ***The effective characteristic impedance of the bus line is matched with the characteristic impedance of the wiring of the motherboard*** (3).

(Specification; page 10, line 23 to page 11, line 8; emphasis added). In contrast, in Moriarty "[o]ne most important feature of such buses is that the effective impedance of the signal propagation paths is well controlled, and one end of the bus is ***terminated to the characteristic impedance of the bus in order to maintain signal integrity.***" (Moriarty; col. 2, lines 19-23; emphasis added). Also, Moriarty states that "[t]he memory module may be formed on a conventional printed circuit card." (Moriarty; col. 4, lines 22-24). Additionally, Moriarty states:

> Cards 144, 156, and 166 typically are printed circuit structures, comprising epoxy-glass-based materials (i.e., FR4) and include one or more conductive (i.e., signal, power and/or ground) layers therein. Other materials may be used for various reasons, including electrical performance, wirability, and thermal performance, but epoxy-glass-based materials are cost-effective and have a CTE that matches that of system board 12 and LGA connectors 142 and 154. Again due to the stringent RAMBUS electrical specifications, the ***signal traces must match the system impedance within ten percent.***

(Moriarty; col. 10, lines 30-39; emphasis added). However, it appears that the disclosure in Moriarty differs from the present invention in that there is no explicit disclosure in Moriarty of a

bus line being a strip line. Therefore, Moriarty does not disclose or suggest all of the features of claim 2. Therefore claim 2 is allowable at least for this reason.

Claims 3, 4, 11, 18, and 19 depend from claim 2 and therefore these claims are allowable for at least the same reasons as claim 2 is allowable.

Additionally, claim 4 recites that ***at least one of the plurality of memory devices is a memory device in which a termination circuit is included***, and that ***the memory device in which the termination circuit is included terminates the end of the bus line***. The Office Action asserts that Moriarty discloses a termination circuit in figure 7, element 116. (Office Action; page 3, lines 6-7). However, element 116 is merely a termination or a termination component according to Moriarty. (Moriarty; col. 8, lines 12 and 16). Since the Examiner asserts that elements 28 disclose the memory devices, and since element 116 is separated from the nearest element 28 on element 104 at least by element 126, which is apparently bus steering means (Moriarty; col. 8, lines 60-61), Moriarty does not disclose or suggest a memory device including a termination circuit, as recited in claim 4. Therefore, for at least this additional reason claim 4 is allowable.

New claims 45-47 depend from claim 2 and are therefore allowable at least for the same reasons as claim 1 is allowable.

New claims 48-50 depend from allowable claim 25 and are therefore allowable at least for the same reasons as claim 25 is allowable.

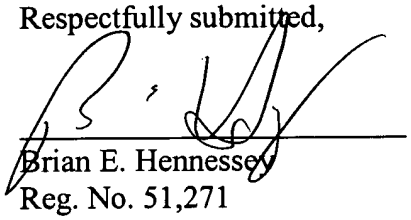
CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that the claims are in condition for allowance. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged on Deposit Account 50-1290.

Respectfully submitted,



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